

2025年臺灣國際科學展覽會 優勝作品專輯

作品編號 100033

參展科別 工程學

作品名稱 Electrical Characterization of MoS₂
Field-Effect Transistors at Cryogenic
Temperatures

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關鍵詞 Transistors、MoS₂、Cryogenic temperatures

作者簡介



我們是建國中學數理資優班的羅睿謙（左）和王秉森（右），很幸運能夠透過獨立研究的機會，到台大電機系進行半導體元件的研究，學習相關知識並進行實作。謝謝李峻實教授細心的指導，以及吳昊陽學長、魏明瑤學長、林沂霈學姐等實驗室學長姐，熱心引領我們進入實驗室參與許多實務研究。也謝謝何宣螢老師及家人的支持與鼓勵，讓我們有機會參與本次國際科展。

研究報告封面

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研究報告

區別：北區

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編號：

（編號由國立臺灣科學教育館統一填列）

摘要

隨著矽基電晶體逐漸微縮，其元件效能將接近其物理極限，二硫化鉬 (MoS_2) 等二維材料藉著其獨特的特性(如寬的能隙、高電流開關比及優異的載子遷移率等)，可作為矽的替代材料用於未來的電子科技應用。本研究旨在製造 MoS_2 的場效電晶體並研究元件之低溫特性。我們成功利用機械剝離法製備並轉移二維 MoS_2 薄膜至二氧化矽/矽基板上，並且製造 MoS_2 場效電晶體，並量測其室溫(300 K)至極低溫(~ 4 K)的電流特性，元件在此溫度範圍中具有優異的特性，能有效地調控電流調控，表現出良好的下閘極控制能力，同時具有低次臨界擺幅及高電流開關比($\sim 10^6$)。在極低的溫度(4 K)下，該電晶體仍能保持良好的運作，顯示出 MoS_2 應用於低功耗且高元件效能的低溫電子元件的潛力。

Abstract

As silicon-based transistors approach their physical limits, 2D materials like MoS_2 with unique electronic properties are considered one of the potential alternatives to silicon for future electronics. In this work, we fabricate a MoS_2 -based transistor and investigate its device performance at cryogenic temperatures, relevant for quantum computing applications. Using mechanical exfoliation, we successfully transfer MoS_2 films on a SiO_2/Si substrate and fabricate transistors. Then we perform electrical measurements from room temperature (300 K) to cryogenic temperatures (down to 4 K), at which the device shows great performance with effective current modulation by bottom gate control, very low subthreshold swings, and high ON/OFF ratios. What is more important is that at cryogenic temperatures, the transistor still performs very well, showing the great potential of MoS_2 for low-power and high-performance cryogenic electronic devices.

I. Introduction

A. Motivation

Over the past six decades, the size of transistors is continuously shrinking to keep up with Moore's Law. However, silicon-based transistor devices are now approaching its physical limits, which poses challenges to preserve their high performance and reliability. Scientists are exploring alternative materials that could provide exceptional characteristics at a nanoscale. One of the most promising categories is 2D materials, as it offers great characteristics for nanoscale device applications, such as their atomic layer thickness of only a few angstroms, which helps to suppress leakage current, carrier scattering, and short-channel effects [1] that conventional silicon transistors face at the nanoscale or angstrom technology node.

Molybdenum disulfide (MoS_2), a member of the transition-metal dichalcogenides (TMD) family, presents outstanding properties such as a large band gap (~ 1.8 eV for monolayer), high ON/OFF ratio for transistors, and exceptional electron mobility [2], which enhances the switching speed of the transistor. Given those advantages, we are interested in a possible application using MoS_2 transistors as cryogenic interface electronics (CIE) for quantum computing, which requires high-performance devices at cryogenic temperatures to reduce heats. Thus far, theoretical work on MoS_2 transistors at cryogenic temperatures was proposed [3], but there were only few experimental results demonstrated. In this work, we investigate the device performance of MoS_2 transistors at cryogenic temperatures ($300 \sim 4$ K) and demonstrate its potential for future applications.

B. Goals

1. Fabrication of a MoS_2 transistor
2. Characterization of MoS_2 transistors at cryogenic temperatures to evaluate its potential for quantum computing applications

II. Literature Review

A. 2D materials

The development of semiconductor transistors has greatly influenced modern worlds for the past six decades. Initially, it played an indispensable role in electronics and communication systems and now almost every device contains transistors! Since the discovery of graphene in 2004 [4], there has been great interest in two-dimensional materials owing to its extraordinary electrical properties. However, graphene cannot be used as field effect transistors (FETs) due to its lack of an intrinsic bandgap [5], making it unattainable to provide distinct ON and OFF states for logic switching. Transition metal dichalcogenides (TMDs), therefore, have become one of the main research focus of scientists due to their tunable bandgaps and other electrical, optical, and mechanical properties. The most common 2D materials have a general formula of MX_2 , where M represents a transition metal and X is a chalcogen. Their electrical state ranges from metallic to insulating states. Group-VI TMDs such as MoS_2 , WSe_2 , WS_2 , and MoSe_2 have gained great attention for their semiconducting properties. [6, 7]

MoS_2 is one of the most promising materials due to its favorable characteristics. MoS_2 is a n-type semiconducting material (with a direct bandgap of 1.8 eV) with electrons as major charge carriers. The molybdenum (Mo) atoms are sandwiched between two layers of sulfur (S) atoms (**Figure (1)**), and those layers are easy to be exfoliated down to monolayers because of the weak van der Waals force bonding between layers. The thickness of a monolayer MoS_2 is only about 6.5 Å. It also has a high mobility of up to $\sim 200 \text{ cm}^2/\text{Vs}$ at room temperature (for a monolayer form), which has high potential to achieve lower power dissipation for future electronic logic devices. [7, 8]

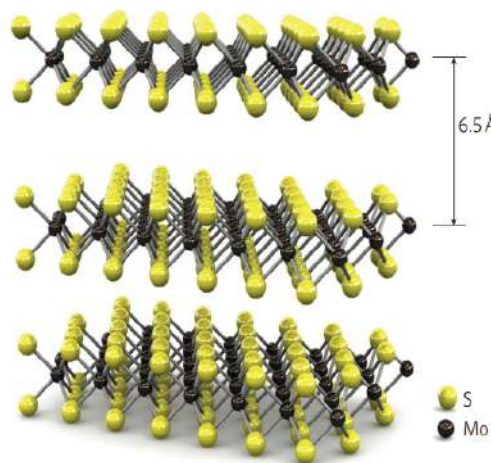


Figure (1) | Structure of MoS_2 (Image source: [9]).

While WS_2 and WSe_2 are also promising materials, both have their own limitations. WSe_2 , for instance, is a p-type material with a band gap of 1.7 eV. Its fabrication is more difficult than that of MoS_2 , resulting in a much slower pace in the development of transistors. Similarly, WS_2 possesses great properties such as a bandgap of 2 eV and a predicted high carrier mobility due to reduced effective mass. However, less attention has been paid compared to MoS_2 . [2, 10].

B. Cryogenic transistors

2D materials have shown great promise for use in cryogenic CMOS (complementary metal-oxide-semiconductor) interface electronics for quantum computing [3]. Conventional CMOS circuits for quantum computing are operated at room temperature, so it requires dedicated wirings to interface with the quantum bits (qubits) housed in a dilution refrigerator at cryogenic temperatures (**Figure (2)**). This approach limits the scalability of qubit systems due to the low thermal budgets of conventional dilution refrigerators. If we integrate both qubit and CMOS systems within the refrigerator, the CMOS power dissipation must be minimized, which requires a reduced operational voltage (V_{DD}).

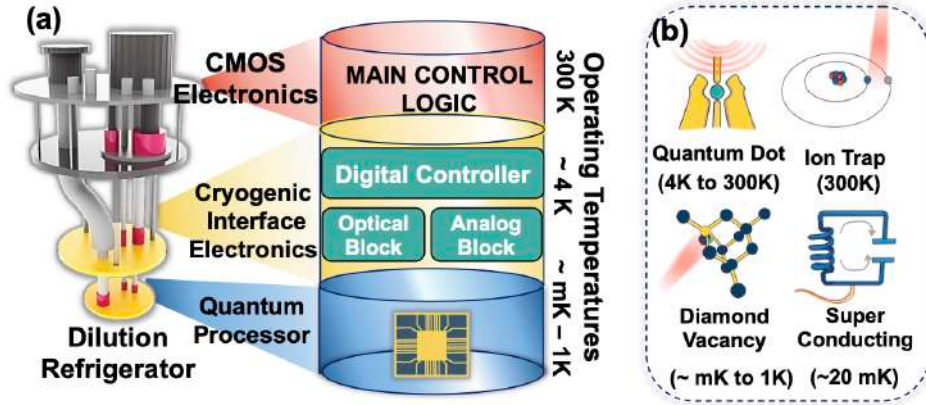


Figure (2) | Schematic diagram of a dilution refrigerator (DR) (Image source: [3]).

Conventional bulk semiconductors like Si, Ge, and GaAs have poor electrostatics and large band-tails that limit the extent of V_{DD} scaling [3]. 2D materials, on the other hand, offer excellent electrostatics due to their ultrathin body and pristine interfaces. This enables a lower V_{DD} and reduction of parasitic capacitance [3]. Moreover, their large bandgaps imply an intrinsic carrier concentration that decays much faster with temperature, hence reducing

junction leakage power at cryogenic temperatures. Owing to the layered nature and low phonon density-of-states (DOS), 2D materials also have short band-tails, thereby allowing the reduction of subthreshold swing (SS) and scaling V_{DD} down to 4 K [3] (Figure (3)).

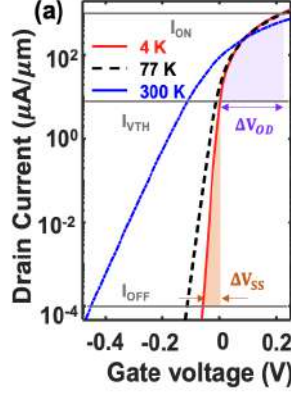


Figure (3) | Device characteristics at CT (Image source: [3]).

Simulation results showed that the performance of 2D material-based FETs surpasses that of Si-based FETs at cryogenic temperatures. A 2D FET shows a lower SS due to their smaller Urbach energies [3]. In addition, for the application of digital and analog circuits like CMOS inverters and low-noise amplifiers, 2D material-based FETs might perform better than Si-based FETs at cryogenic temperatures, owing to the capability to meet with the requirement of drive current at an ultra-low voltage of 0.2 V [3]. Another advantage of 2D materials lies in their potential to reduce noise, a critical factor that affects qubit decoherence in quantum computing. The lower band-tails of 2D materials compared to Si contribute to lower shot and flicker noise at cryogenic temperatures, the latter being the most dominant source of phase decoherence in qubits. This is very important in terms of preserving the fidelity of control pulses and read signals in cryogenic quantum computing systems [3].

III. Experiment

The flow chart of the experiment process is shown in **Figure (4)**.

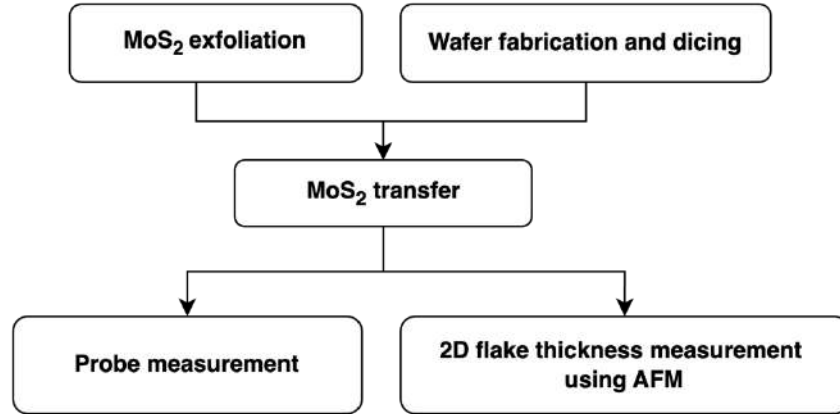


Figure (4) | Flow chart of experiment process.

A. Material preparation

1. Exfoliation

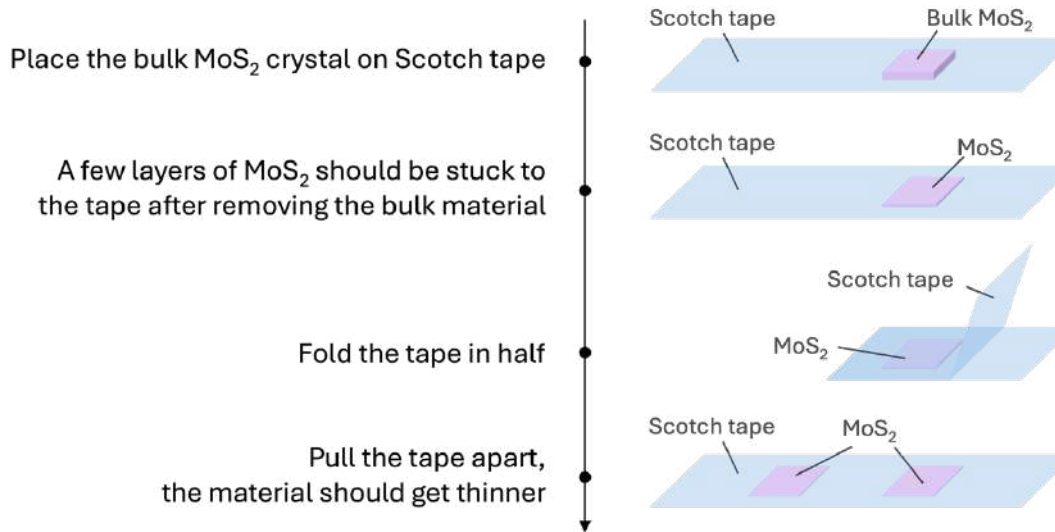


Figure (5) | Mechanical exfoliation process (dry exfoliation method).

We used a dry exfoliation method (or Scotch tape method) to exfoliate thin MoS₂ films from a bulk material (**Figure (5)**). A piece of Scotch tape was first used to peel off material from a chunk of bulk MoS₂. The tape was then folded and pulled apart carefully. This was operated numerous times. Each time the tape was pulled apart, the material gets thinner, and eventually result in a 2D plane.

2. Surface characterization of 2D flakes

AFM (Atomic force microscopy) was used to determine the thickness of our 2D flakes (**Figure (6)**). When the sharp tip on a cantilever scans the sample, it is drawn to the surface due to the van der Waals force with surface atoms, resulting in the deflection of a laser beam focused on the cantilever. The deflection signal is recorded by a diode, varying with the extent of the laser deflection, and the controller commands the piezoelectric actuator to move across the surface through the actuation circuit, forming the scan image during the process. Ultimately, the image displays fluctuations of the surface height, helping us determine the thickness of our sample. [11] The AFM image our MoS₂ flake is shown in **Figure (7)**. The height of the MoS₂ flake is approximately 42 nm.

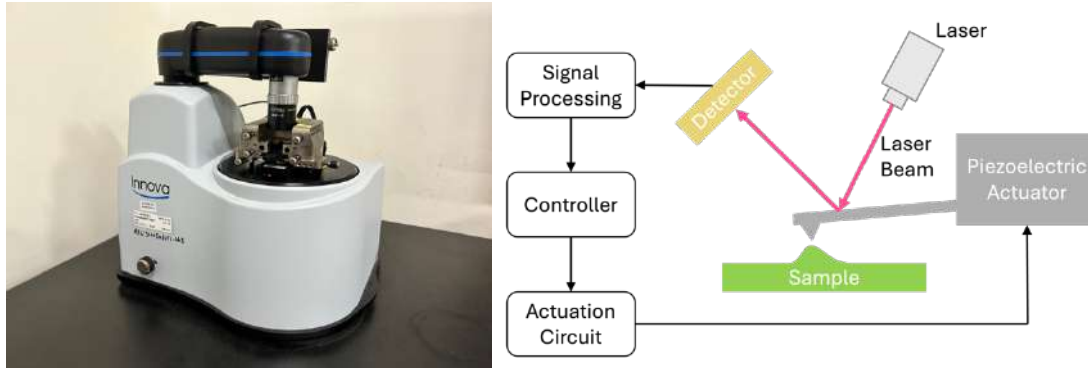


Figure (6) | A photo of an AFM equipment (left) and a schematic diagram of its system (right).

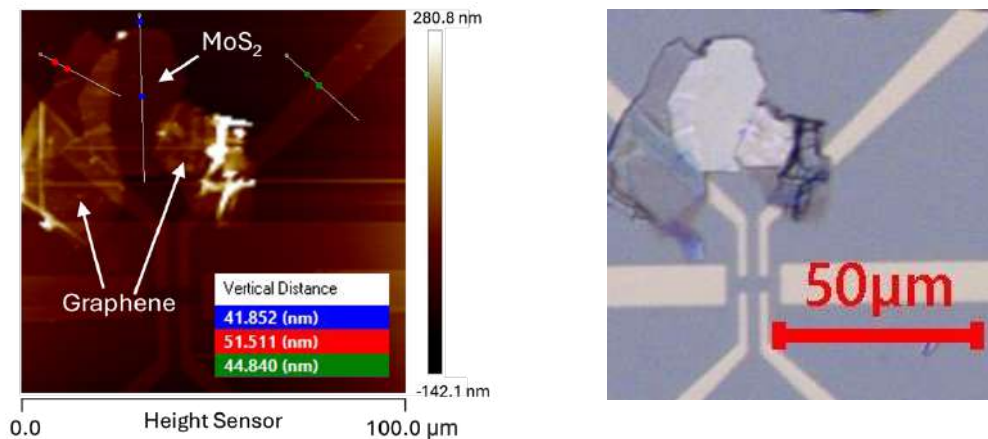


Figure (7) | An AFM image of a MoS₂-based transistor (left) and its optical microscopic image (right).

B. Device fabrication

1. Preparation of Si/SiO₂ substrates

(Due to safety considerations, steps a, c, and d are conducted by experienced lab members.)

Process flow of wafer fabrication

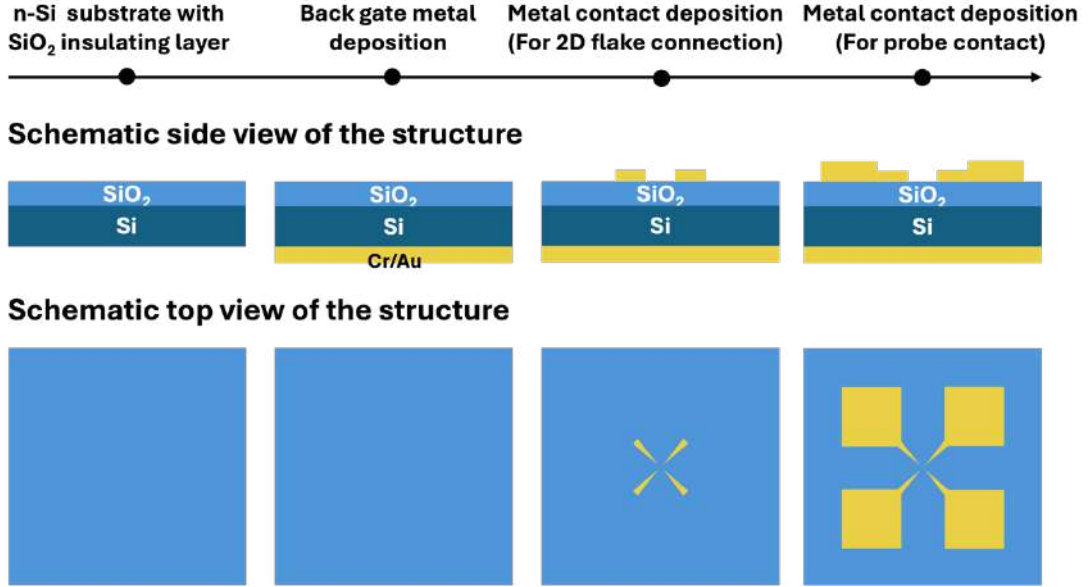


Figure (8) | Process flow of wafer fabrication.

- A 15-nm SiO₂ insulating layer was deposited onto a highly phosphorus-doped n-Si substrate at TSRI (Taiwan Semiconductor Research Institute).
- The wafer was diced into small pieces. It is done by applying force to the wafer with a diamond pen. It will then crack along its crystal plane in a perfectly straight line.
- Chromium (Cr) and gold (Au) were deposited onto the back of the substrate, acting as the back gate of the transistor (**Figure (8)**).
- After performing photolithographic and lift-off steps (**Figure (9)**), metal contacts were formed on the surface of the substrate (**Figure (8)**), serving as the connection between 2D flakes and measurement probes.

Photolithography and Lift-off Process Flow

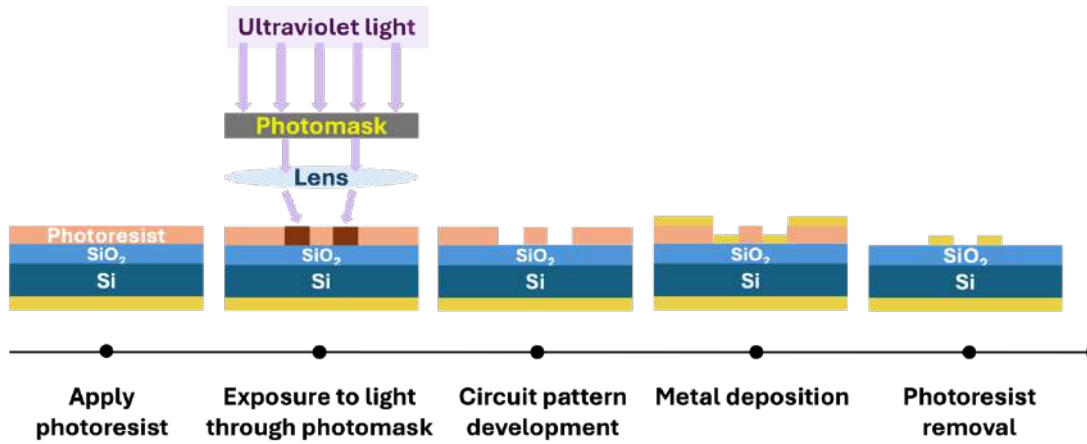


Figure (9) | Process of photolithographic and lift-off steps.

2. Transfer of 2D materials

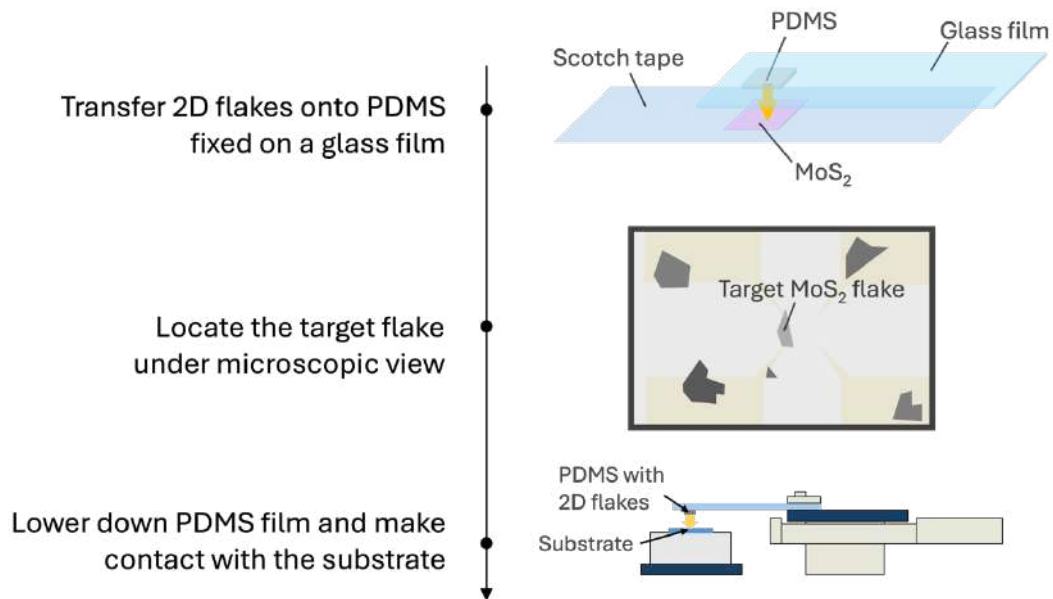


Figure (10) | 2D materials transfer process.

- A silicon wafer was loaded into the glove box and placed under the microscope.
- Inside the glove box, some of the 2D flakes were then transferred onto a thin film of Polydimethylsiloxane (PDMS) (**Figure (10, 11)**) for a better and more convenient transfer process.



Figure (11) | Thin film of PDMS on a glass slide (left), and the exfoliated MoS₂ on a strip of Scotch tape (right).

- c. After the film of PDMS was fixed onto a mechanical arm and adjusted under the view of the microscope, we then located the 2D flake that will later be transferred (**Figure (10)**).
- d. The transfer of 2D flakes was done by lowering down the PDMS film, bringing it into contact with the substrate (**Figure (10, 12)**). The flake should contact with two electrodes that functions as the drain and source of the transistor, after the PDMS film is lifted. [12, 13]



Figure (12) | Glove box for 2D transfer system (left), and a schematic structure of the system.

3. Electrical measurement by a probe station

a. Measurement at room temperature

- (1). The transistor device was positioned into a probe station (**Figure (13)**) and contacted with probes. The door to the probe station needs to be closed to create a dark environment, preventing light injecting into the devices to generate electrons and holes from measurement results.
- (2). A semiconductor device parameter analyzer (B1500) that is connected to the probe station was used to conduct the electrical measurement (i.e. current vs. voltage).

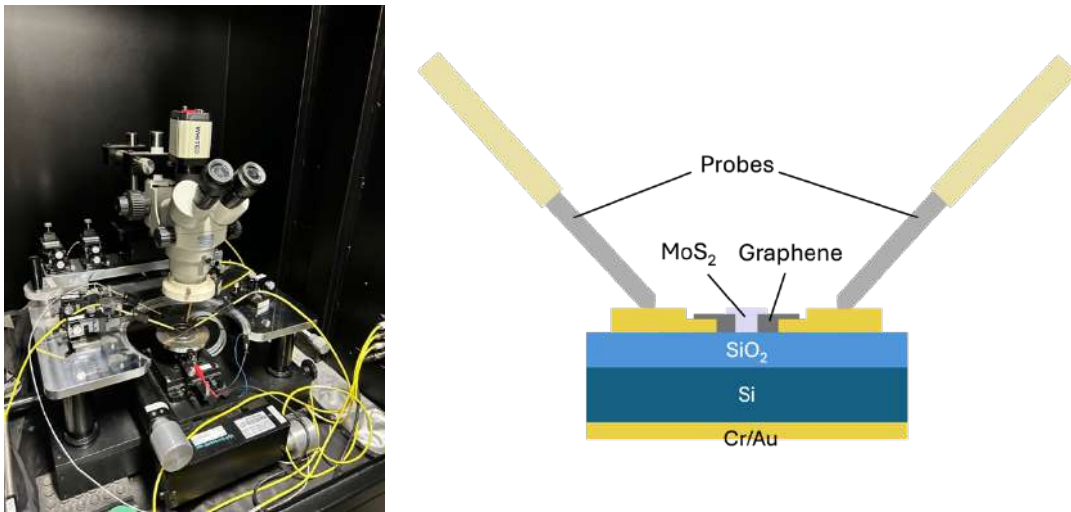


Figure (13) | Probe station (left) and a schematic diagram of the setup (right).

b. Cryogenic measurements

Cryogenic measurement was conducted with CRX-4K (**Figure (14)**), a specialized probe station. A He⁴ compressor was used to lower the temperature to 4 K, and a PID-controlled heater to adjust the temperature (from 4 K to 300 K). The steps of electrical characterization were the same as that used at room temperature.

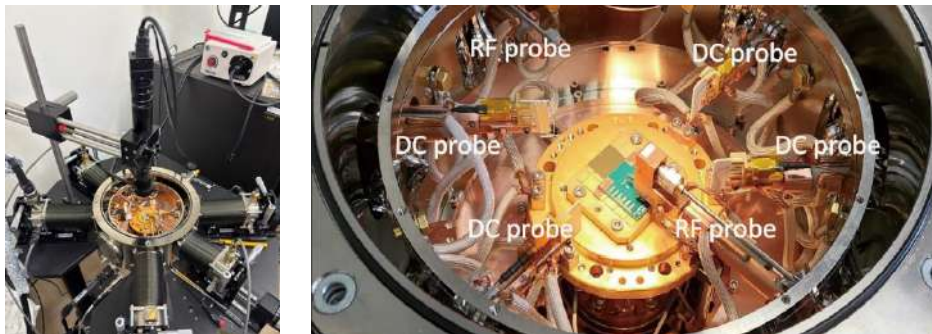


Figure (14) | Photos of a CRX-4K equipment for cryogenic measurement.

IV. Results and Analysis

Figure (15) shows the microscopic and schematic image of a MoS₂ transistor. The following results are the measurement results of this device.

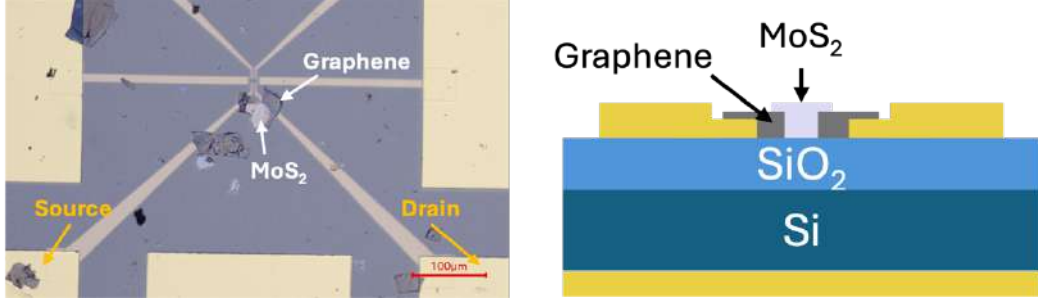


Figure (15) | Microscopic image (left) and a schematic of side-view (right) of a MoS₂-transistor.

A. Electrical characteristics at room temperature

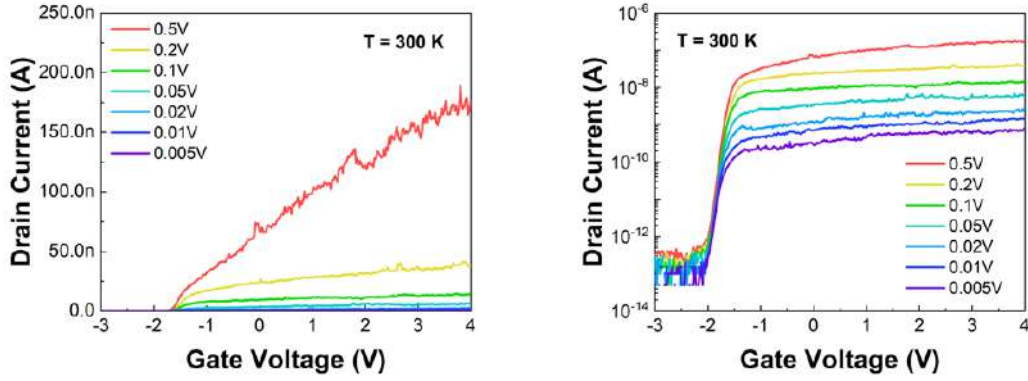


Figure (16) | I_d - V_g curve at room temperature in a linear (left) and logarithmic (right) scale. Curves were measured at different drain biases.

The electrical characteristics of the MoS₂ transistor at room temperature is shown in **Figure (16)**. For a fixed V_{ds} , the drain current is fairly close to zero when the gate voltage is smaller than the threshold voltage (V_{th}). There is a steady trend of increasing drain current with the gate voltage once V_g is larger (more positive than) V_{th} , as the MoS₂ flake exhibits n-type characteristics. In addition, current increases with V_{ds} , as expected for a transistor. This means that both the gate voltages and the drain-to-source voltages can modulate the current in our device effectively, indicating that the device works properly. The graph on the right in **Figure (16)** is presented in a logarithmic scale, which enables us to better extract the ON/OFF current ratio and subthreshold slope more clearly. The large difference between the ON and OFF current indicates excellent gate control over the MoS₂ channel and low leakage current in the OFF state, which is crucial for low power

electronics. The subthreshold slopes are very steep across different V_{ds} , where the current changes sharply as the gate bias is close to the threshold. This implies that a lower voltage is needed to reach the ON state, which is desirable for low-power devices to save power.

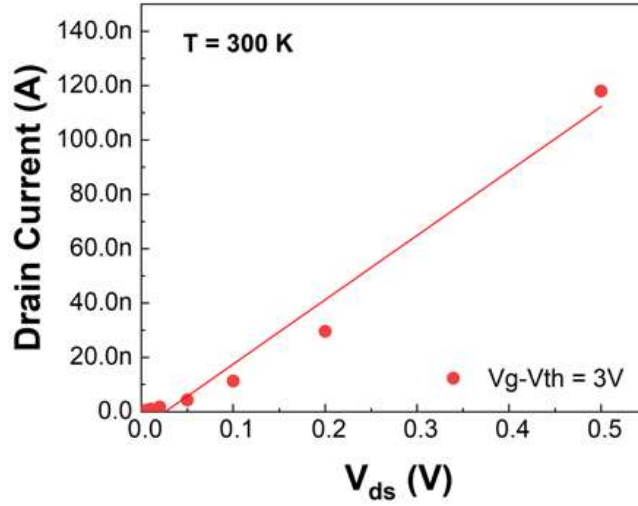


Figure (17) | Drain current (I_{ds}) vs. voltage (V_{ds}), under a fixed overdrive voltage ($V_g - V_{th}$) of 3 V at room temperature

Figure (17) shows the drain current under an overdrive voltage ($V_g - V_{th}$) of 3V, which corresponds to the triode region, where the device is at “ON” state and behaves like a resistor. The drain current of our device is linearly proportional to V_{ds} , which suggests that our device was operated normally in the triode region.

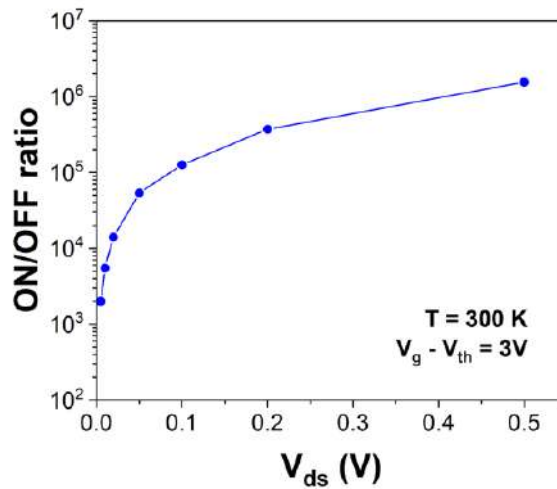


Figure (18) | ON/OFF current ratio vs. voltage (V_{ds}) at room temperature under an overdrive voltage of 3 V.

The ON/OFF current ratio under an overdrive voltage of 3 V is plotted in **Figure (18)**. It increases exponentially as V_{ds} increases from 5 mV to 0.5 V. Even at lower V_{ds} values, the ON/OFF current ratios are still high ($10^3 \sim 10^4$), which is promising for low-power applications.

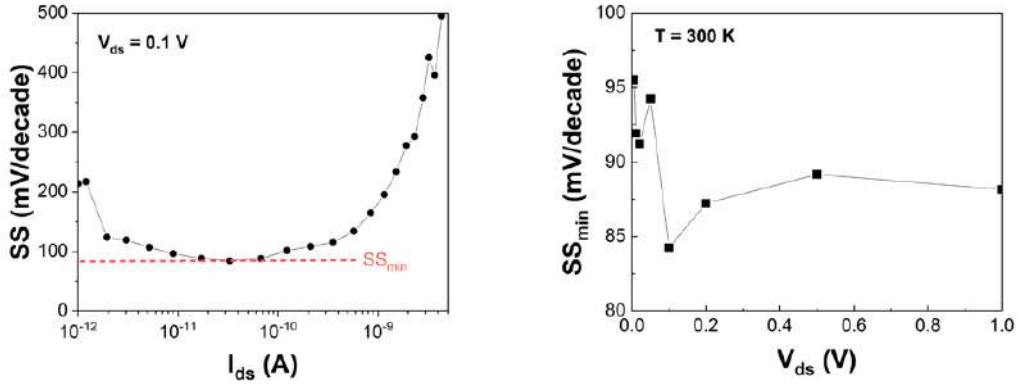


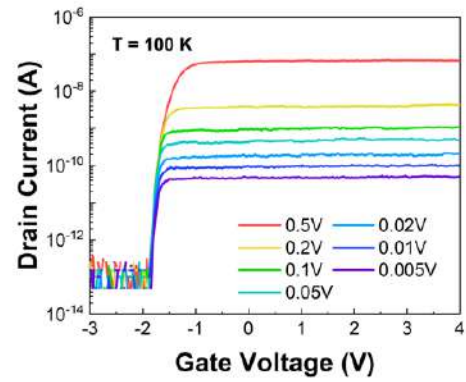
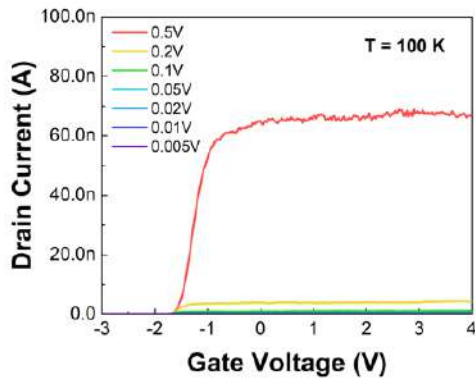
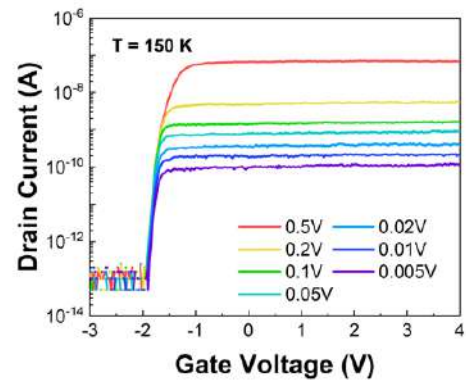
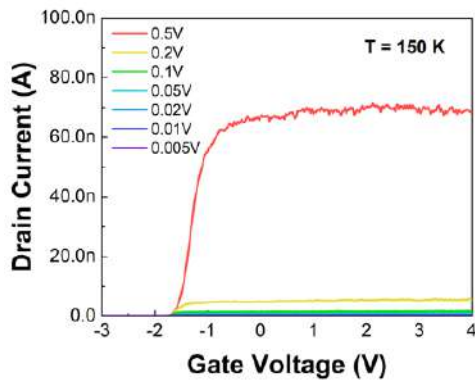
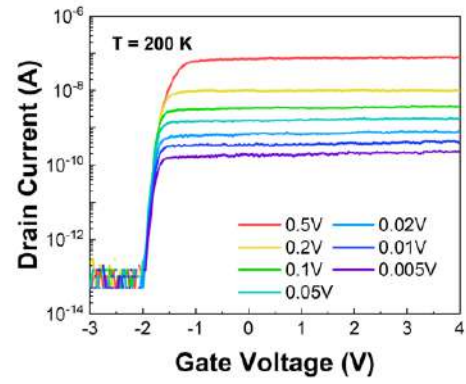
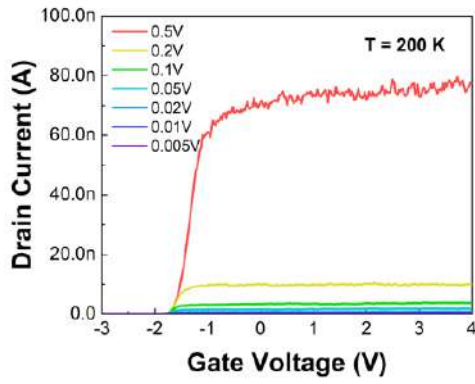
Figure (19) | Subthreshold swing vs. drain current (I_{ds}) under a drain-to-source voltage of 0.1 V (left). The minimum SS value (SS_{min}) vs. drain voltages (V_{ds}) (right).

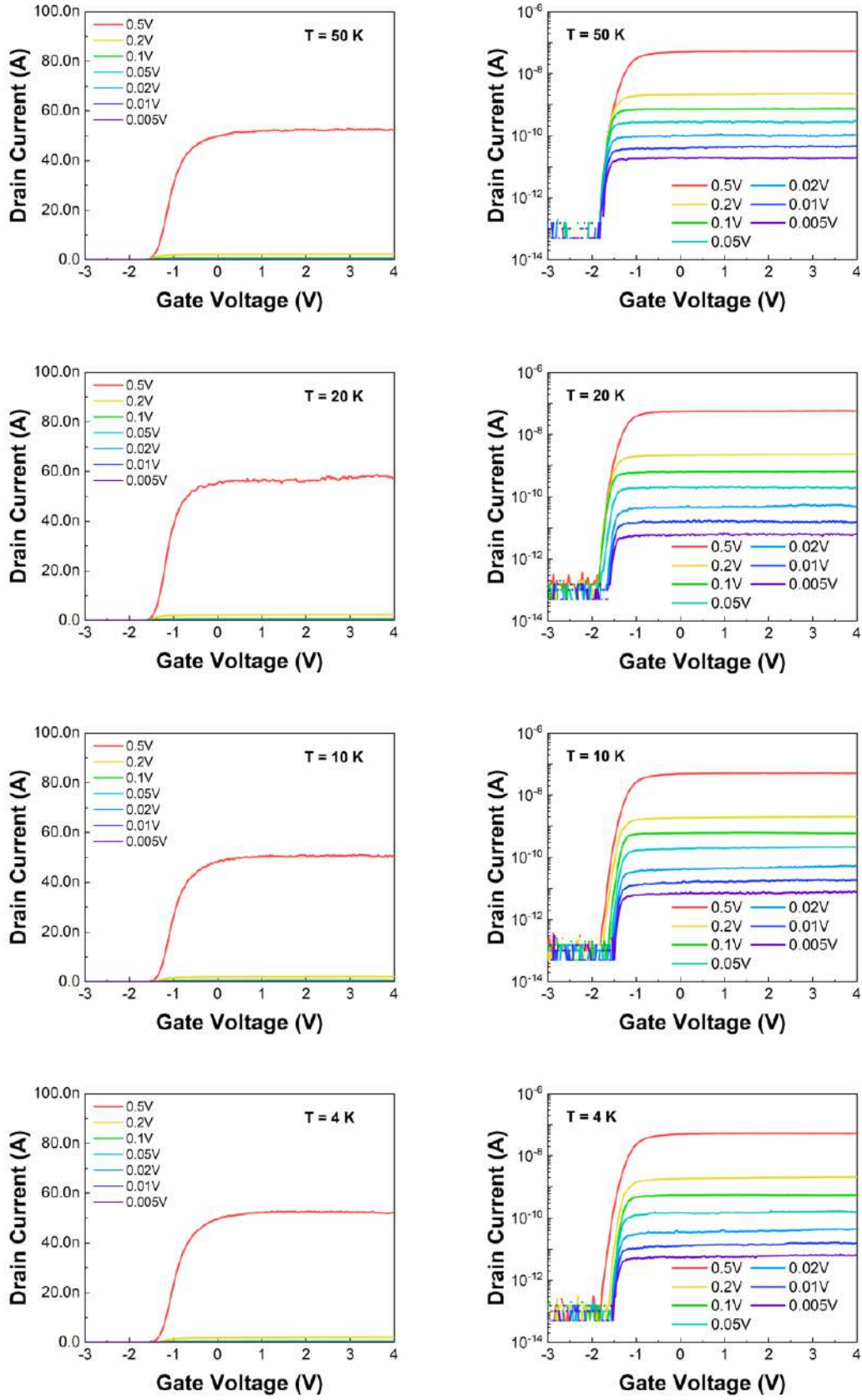
Figure (19) shows the subthreshold swing (SS) across several decades of drain current values at V_{ds} of 0.1 V. The SS is calculated using the following formula [14]:

$$SS = \frac{d(V_g)}{d(\log(I_{ds}))}$$

Initially, the subthreshold swing decreases as the drain current increases, reaching a minimum value of approximately 84.3 mV/decade, before it rises again as the current values go higher due to the leakage. The minimum SS is a key factor in determining the performance of a transistor, due to its implications of how efficiently the device can be switched. Thus, a low SS value of 84.3 mV/decade is desirable. We then extracted the minimum SS at different V_{ds} values (**Figure (19)**). The minimum SS is higher at a very small V_{ds} . The dependence of the SS on the drain voltage requires further investigation.

B. Electrical characteristics at cryogenic temperatures





Figure(20) | I_d - V_g curve at temperatures from 200 K to 4 K in linear (left) and logarithmic (right) scales.

Figure (20) displays the $I_d - V_g$ curves of our device across a wide range of temperatures (200 K to 4 K). Compared to the results at room temperature, the drain current increase more abruptly with the gate bias at the subthreshold regime. The ON current of the device at lower temperatures also remains almost constant compared to the case at room temperature. In addition, the curves become smoother as the temperature decreases, implying the reduced interference from thermal noise, leading to a more stable carrier transport in the device channel.

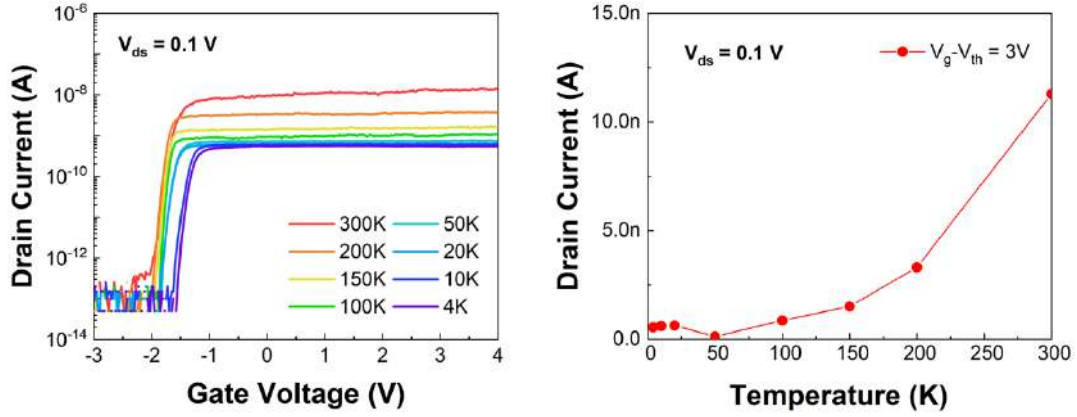


Figure (21) | The $I_d - V_g$ curves from 300 K down to 4 K at $V_{ds} = 0.1$ V (left) and drain current vs temperature at $V_{ds} = 0.1$ V under the overdrive voltage of 3 V (right).

The $I_d - V_g$ curves from 300 K down to 4 K is shown in Figure (21, left). It shows a general decrease in the ON current with temperature. **Figure (21, right)** shows an increase in drain current with temperature at an overdrive voltage of 3 V in the triode region. At lower temperatures higher mobility is often predicted due to the suppressed lattice vibration effects on the carrier transport [15]. Our devices show the opposite trend as a conventional Si FET [16], which might be due to the ineffective carrier accumulation in the MoS₂ channel. Further investigation will be required.

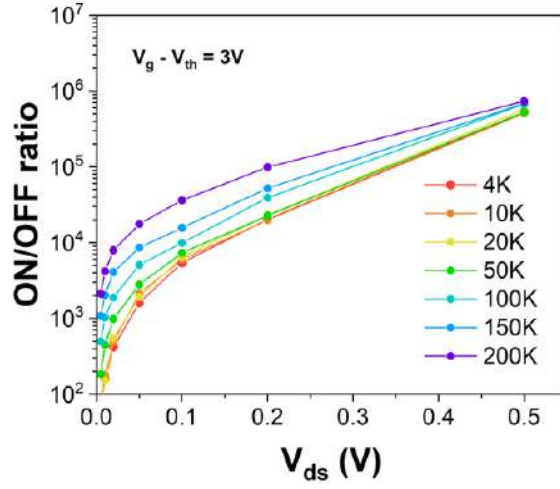


Figure (22) | Plot of current ON/OFF ratio vs. voltage (V_{ds}) at various temperatures.

In **Figure (22)**, we present the ON/OFF ratio values as a function of V_{ds} across a wide range of temperatures. The ON/OFF ratios increase exponentially with V_{ds} , with a highest value of $\sim 10^6$. However, it does decrease at lower temperatures, possibly due to carrier freeze-out, which can also explain the lower currents at deep cryogenic temperatures.

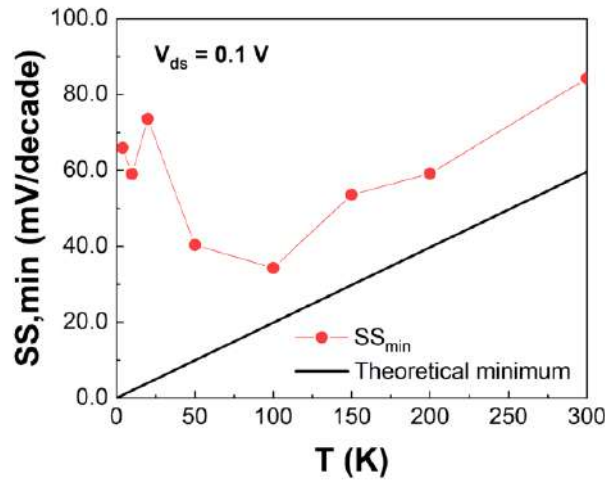


Figure (23) | Minimum SS (SS_{min}) vs. temperature at $V_{ds} = 0.1$ V

Figure (23) shows the minimum SS across different temperatures at $V_{ds} = 0.1$ V. The solid line plotted in the graph represent the minimum theoretical value of the subthreshold slope, calculated using the equation:

$$SS = \ln(10) \cdot \frac{kT}{q} \left(1 + \frac{C_d}{C_{ox}} \right) \quad [17]$$

where k is the Boltzmann constant, T stands for the temperature measured in Kelvin, q is the elementary charge, C_d and C_{ox} are the capacitance of the depletion layer and gate-oxide. The minimum SS shown starts out with 84.3 mV/decade at 300 K and decreases linearly as the temperature is reduced, reaching the lowest of 34.3 mV/decade at 100 K. However, when the temperature continues to drop, the minimum SS values increase again. The results could be attributed to reduced influence of thermal energy at lower temperatures, thus making the existence of band tails the dominant factor that impacts SS_{min} . Since the band tail energy is independent of temperature, the results at cryogenic temperatures no longer follow the Boltzmann limit.

V. Conclusion

In summary, we fabricate a transistor based on mechanically exfoliated MoS₂ and investigate its electrical characteristics. At room temperature, our device exhibits great properties such as high ON/Off ratios and steep subthreshold slopes, which indicates the well-functioning of our device and its ability to control the current efficiently. The minimum SS value increases at deep cryogenic temperatures with the lowest value of 34.3 mV/decade at 100 K.

VI. Future Work

We have demonstrated the high switching efficiency and good current control MoS₂-based devices. In the future, we can explore how to further improve the performance of our device at lower temperatures, such as the saturated subthreshold swing at deep cryogenic temperatures (< 10 K). By overcoming such limitations, we will be able to take a step closer to MoS₂ transistors and utilize the advantages of 2D materials to reduce power consumptions.

VII. Reference

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【評語】100033

本作品嘗試製造基於 MoS₂ 的電晶體並評估其在低溫下的性能。評估實驗中可能出現的變化。

1. 雖然有描述關於剝離、表面表徵與元件製造的程序，但應該更完整的討論關鍵步驟：二維材料的轉移，以評估實驗中可能出現的變化。
2. 僅製作一個元件尚無法論述實驗的再現性與可能的誤差。
3. 元件設計上，應更清楚的論述 graphene 層的作用與影響為何、如何確保 graphene 只包覆於電極位置而不互相接觸產生漏電流通道、元件製作與結果的再現性等。
4. 雖然海報中有較大倍率的影像，但建議作品內應清楚呈現各單元的尺寸，如 gap 寬度、graphene 層數，覆蓋面積、MoS₂ 厚度等等，均是應報導的元件重要基本參數。
5. 各層與電極的貼附性如何？若重複程序製作新的元件時，是否有相同的結果？